MAPPER

Model-based Adaptive Product and Process Engineering

Work Package 2

Evatronix & advICo Use Case:

Collaborative IP-based SoC design

Wojciech Sakowski – Evatronix President & CSO

Presentation Outline

- Short overview of Evatronix & advICo profiles
- use case objectives & our expectations: collaborative IP-based SoC design
- Achievements
  - IP-based SoC design
  - organizational growth
- Ideas on exploitation of MAPPER results for growing Evatronix and advICo businesses

WP2 collaborative network

Evatronix history & today

- **Evatronix S.A. was founded in 1991**
  by Wojciech Sakowski
  and Wlodzimierz Wrona
- It has been operating since then
  as a value added reseller of CAD & EDA solutions…
  reaching in recent years
  one of the leading positions
- TEMPUS project **S_JEP–09151–95**
  - Managed by W. Sakowski
    at Silesian University of Technology in Gliwice between 1995 and 1998
  - cooperation with universities in Paris and Tuebingen
  - Aimed at extending existing curricula with teaching of modern electronic design technologies
    (HDL, ASICs..)
  - Made properly trained graduates available to start in 1997
    electronic virtual component (IP cores) business at Evatronix

- **Electronic Design Department nowadays**
  - brings more than 45% of company turnover
  - employs 45+ designers
    (most in R&D)
  - and 6 -10 interns each year
  - Cooperation with Polish technical universities
  - **ca. 200 licenses sold, interesting list of licensees**
    (Sharp, Toshiba, Spansion, Siemens/Tennessee, ZMD)
  - **Growth of IC design services**
    (AustriaMicroSystems, Yogitech, FingerPrintCards…)

advICo overview

Foundation	August 2000 by Dr. Günter Grau, Dr. Christoph Scheytt
Spin-Off	From Ruhr-University Bochum, Germany Institute for Integrated Circuits
Business Model	Design House & IP Provider
Product Focus	Analog/Mixed-Signal ASIC Design and Services Semiconductor IP, Design Kits
Employees	4
Cooperations	IHP, AWR, Mergeoptics, Ruhr-University Bochum
Customers	IHP, TI Germany, Bosch, Rohde&Schwarz, Mergeoptics, Enpirion, Greatech, Communicant etc.

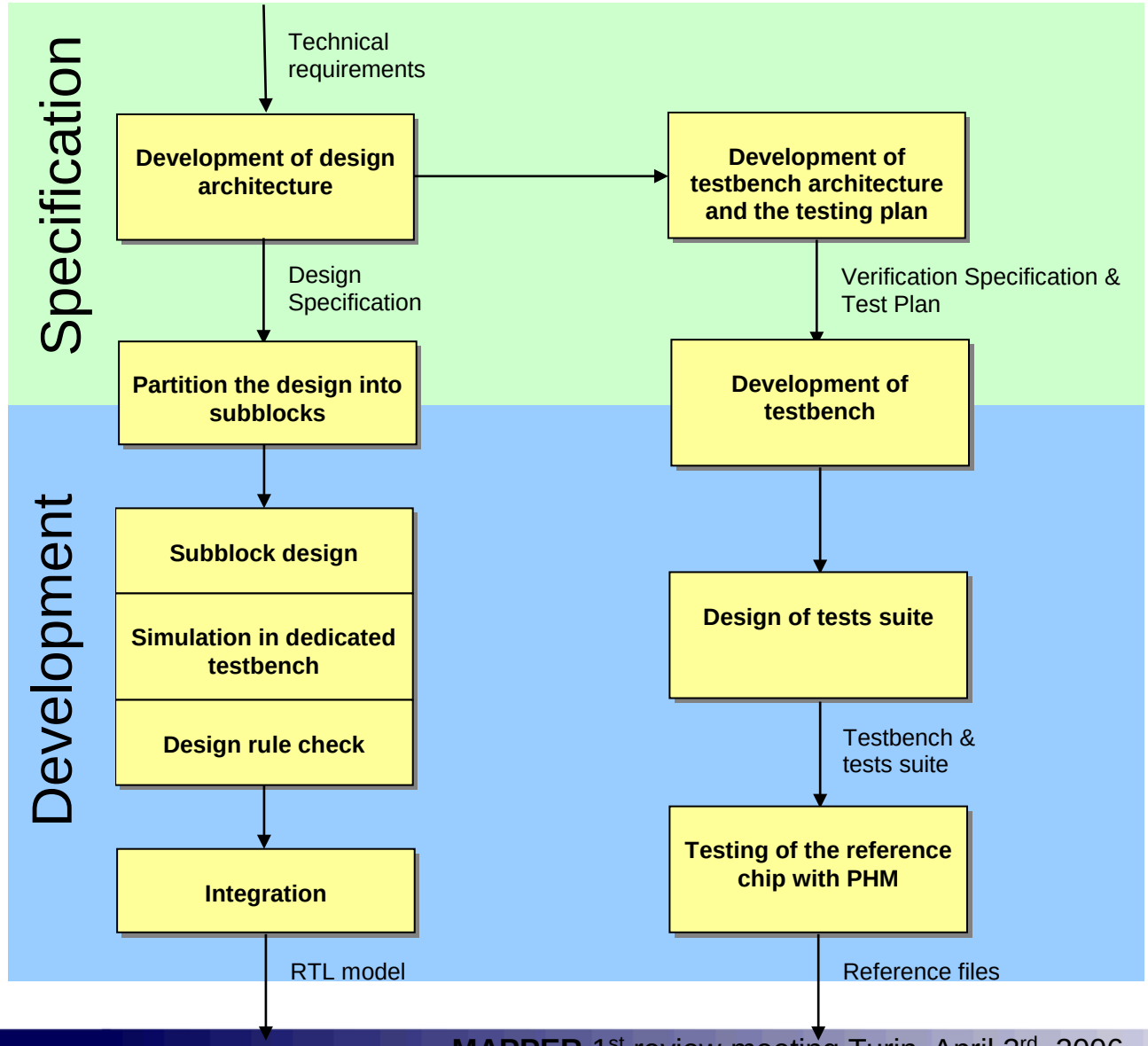
WP2 General Objectives & our expectations

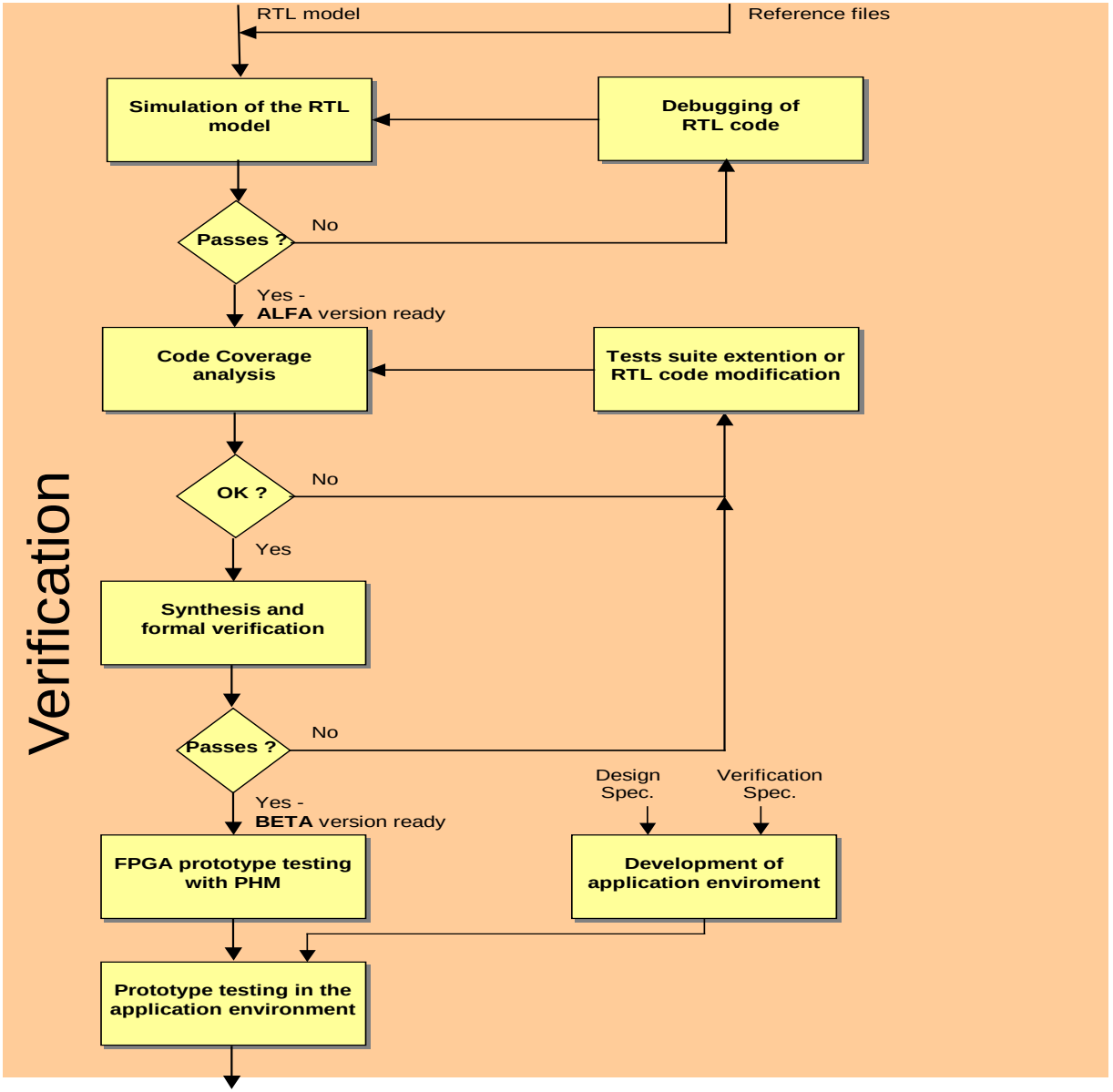
- General objectives (from DoW)
  - knowledge-based and network-based design processes and development,
  - re-use of knowledge-enhanced components,
  - management and protection of product know-how in the network context,
  - methodologies for collaborative engineering with enabling distributed engineering environments, and
  - quality assurance procedures
- Our initial expectations
  - Development of a mixed-signal IP core or/and possibly an Integrated Circuit containing it
  - Setting up an IT infrastructure to support cooperation with a distant engineering team (at customer's site)

Use-case achievements up to date

- **Technical**
  - Current design practices have been captured at Evatronix & advICo (company's main design flow)
  - The objectives of the common design have been detailed and challenges identified
  - Design process model is being built in METIS
- Business
  - Field study at Evatronix held in November 2005 brings valuable observations and requirements
  - Process modeling seminar & Balanced Scorecard seminar held at Evatronix in March 2006
  - business process modeling (with a focus on USE CASE subject) of the Evatronix & advICo with METIS started

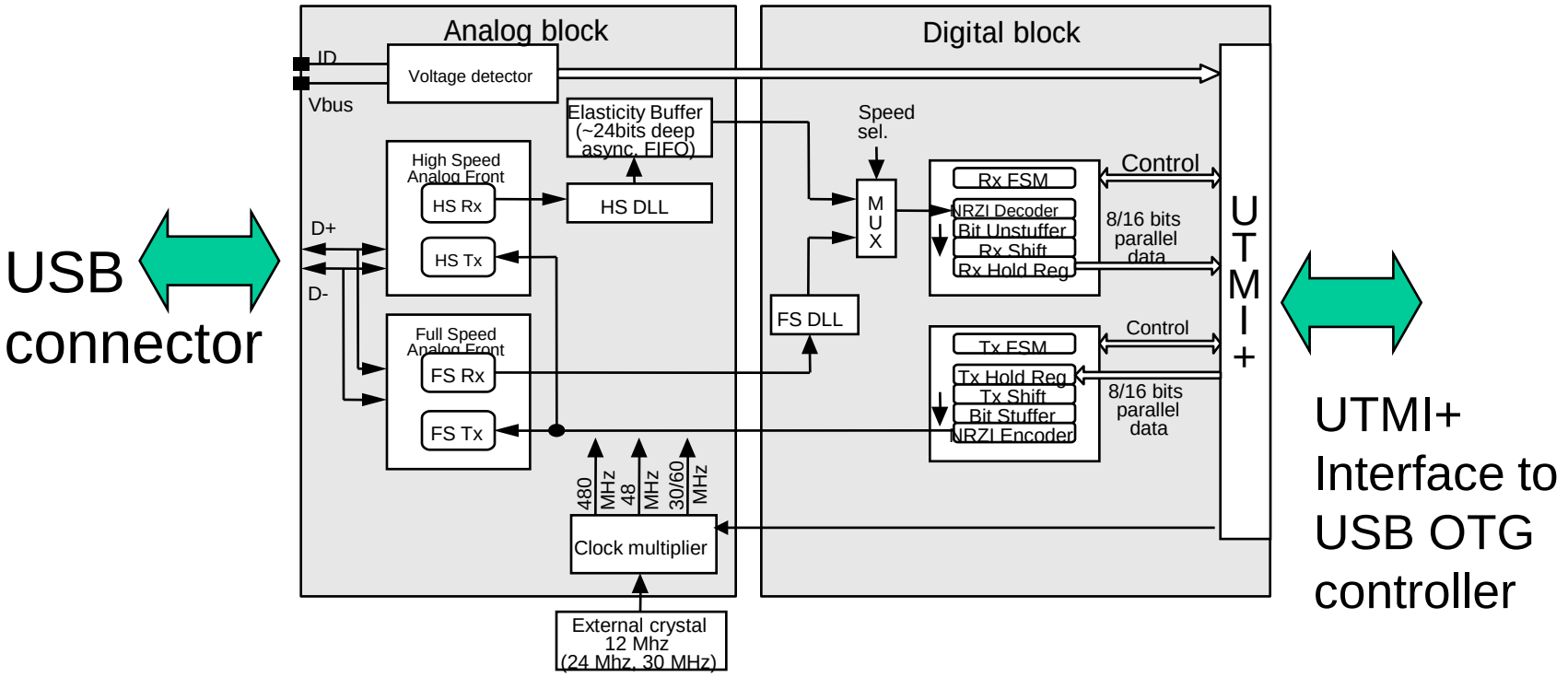
IP-based SoC design




RTL model
Reference files
Simulation of the RTL model
Debugging of RTL code
Passes ?
No
Yes -
ALFA version ready
Code Coverage analysis
Tests suite extention or RTL code modification
OK ?
No
Yes
Synthesis and formal verification
Passes ?
No
Design Spec.
Verification Spec.
Yes -
BETA version ready
FPGA prototype testing with PHM
Development of application enviroment
Prototype testing in the application environment
Verification

IP-based SoC design
- Product (USB OTG PHY) -

- Within the scope of MAPPER WP2,
  Advico and Evatronix develop the USB High Speed OTG Transceiver (PHY, physical layer) IP core with UTMI+ interface.

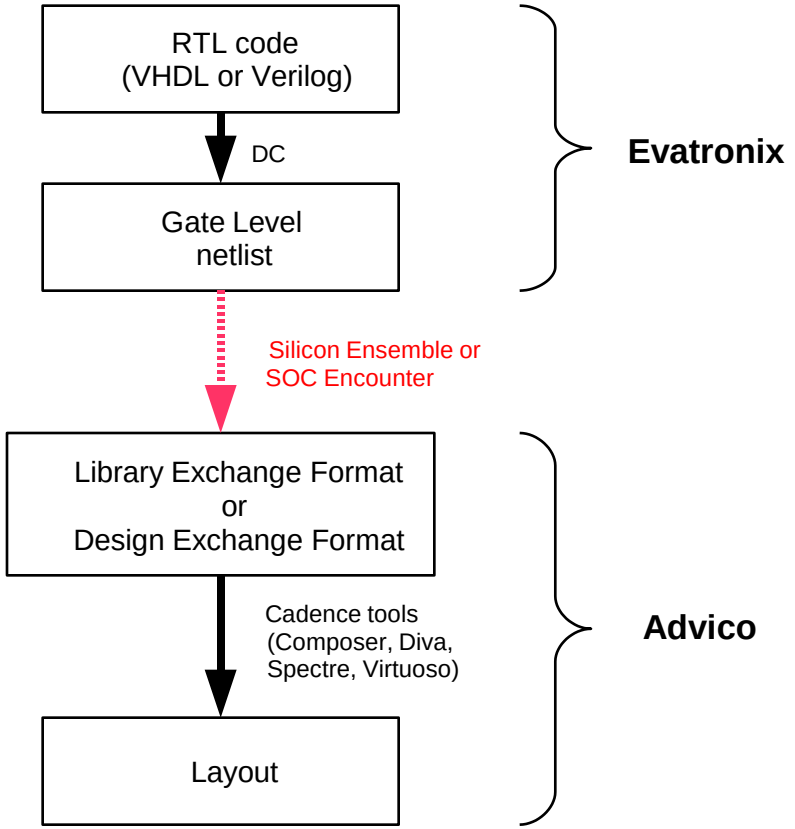


Challenges involved in collaborative design

- Integration of distributed human and technical resources
  - Human resources
    - Engineers in separate geographic locations
    - Different background and organizational culture
  - Technical resources
    - EDA tools
    - IP components
    - design flows

Open issues - broken design data flow?

Evatronix can export component netlist in Verilog, but this is not the format
Advico can directly import.



Use-case achievements up to date

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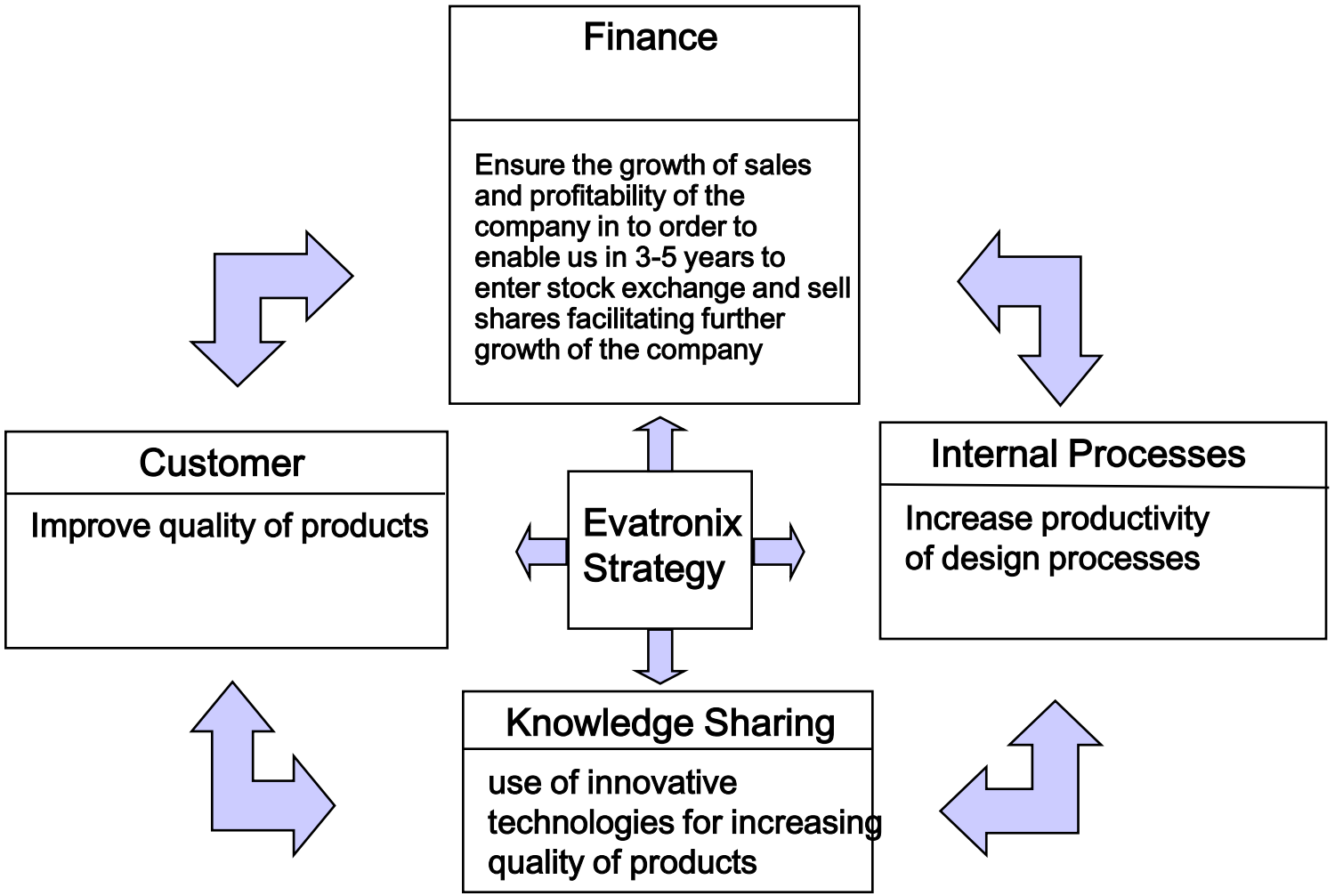
  - The objectives of the common design have been detailed and challenges identified
  - Design process model is being built in METIS
- **Business**
  - Field study at Evatronix held in November 2005 brings valuable observations and requirements
    - **OBSERVATION: Engineering culture far supersedes business management maturity**
  - Process modeling seminar & Balanced Scorecard seminar were held at Evatronix in March 2006
  - business process modeling of the Evatronix & advICo with METIS started

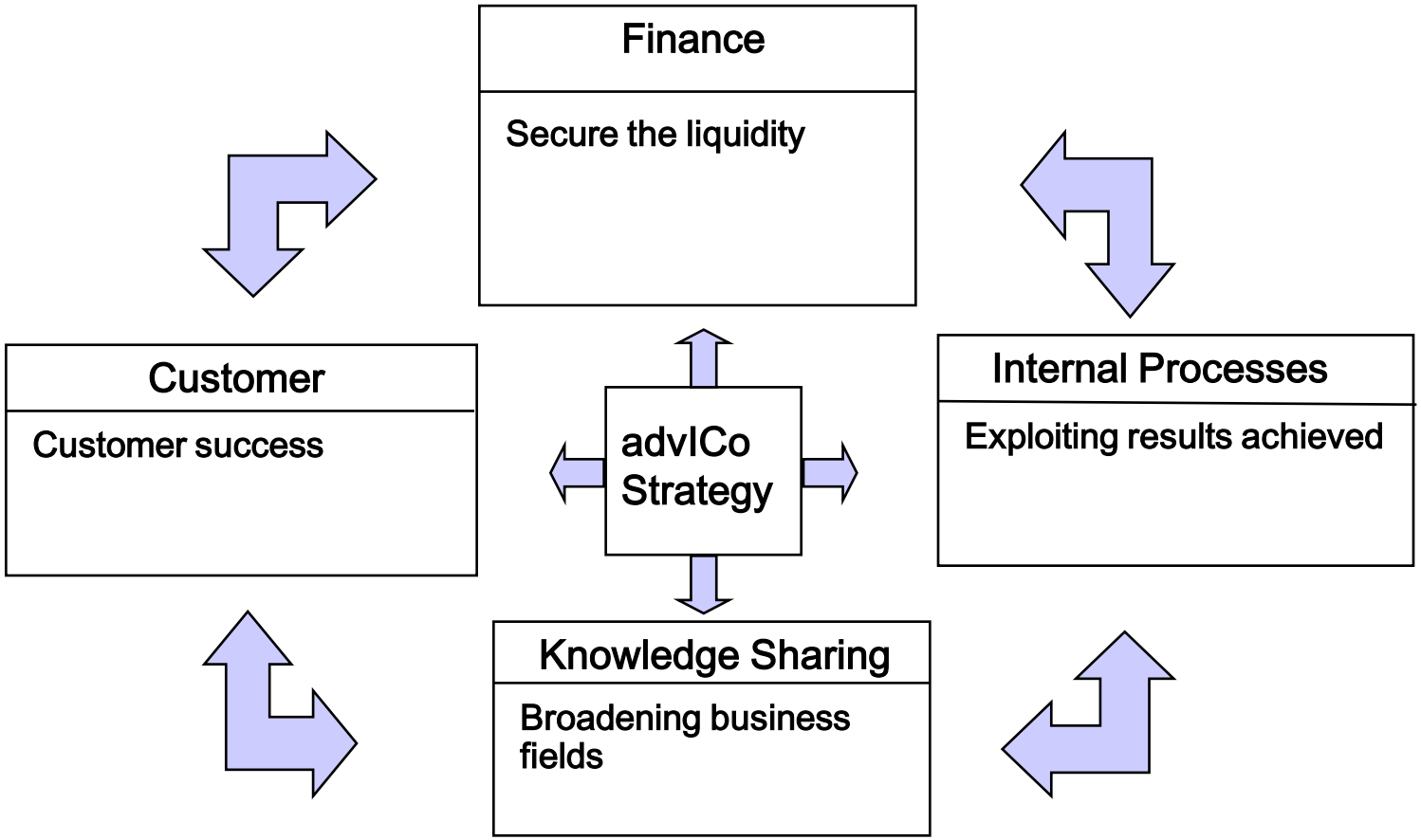
How can we use MAPPER framework to improve Evatronix business practices ?

- Process modeling
  - excellent support for planned organizational changes (from *engineering–focused* to *market–focused* management)
  - process map restructuring before scheduled QMS recertification for compliance to ISO 9000 standard
  - vast deployment of IT tools supporting business processes planned for 2006-2007
    - CRM, EPM, intranet / knowledge repository, extending accounting system to support budgeting & controlling
    - our IT manager responsible for process modeling with METIS
- Introduction of Balanced Scorecard
  - use of BS in defining MAPPER related goals & indicators
  - binding strategic development vision with operational plans in a systematic way (definition of perspectives, goals & subgoals & definition of indicators and ways to measure them)

BS view of Evatronix Business Objectives



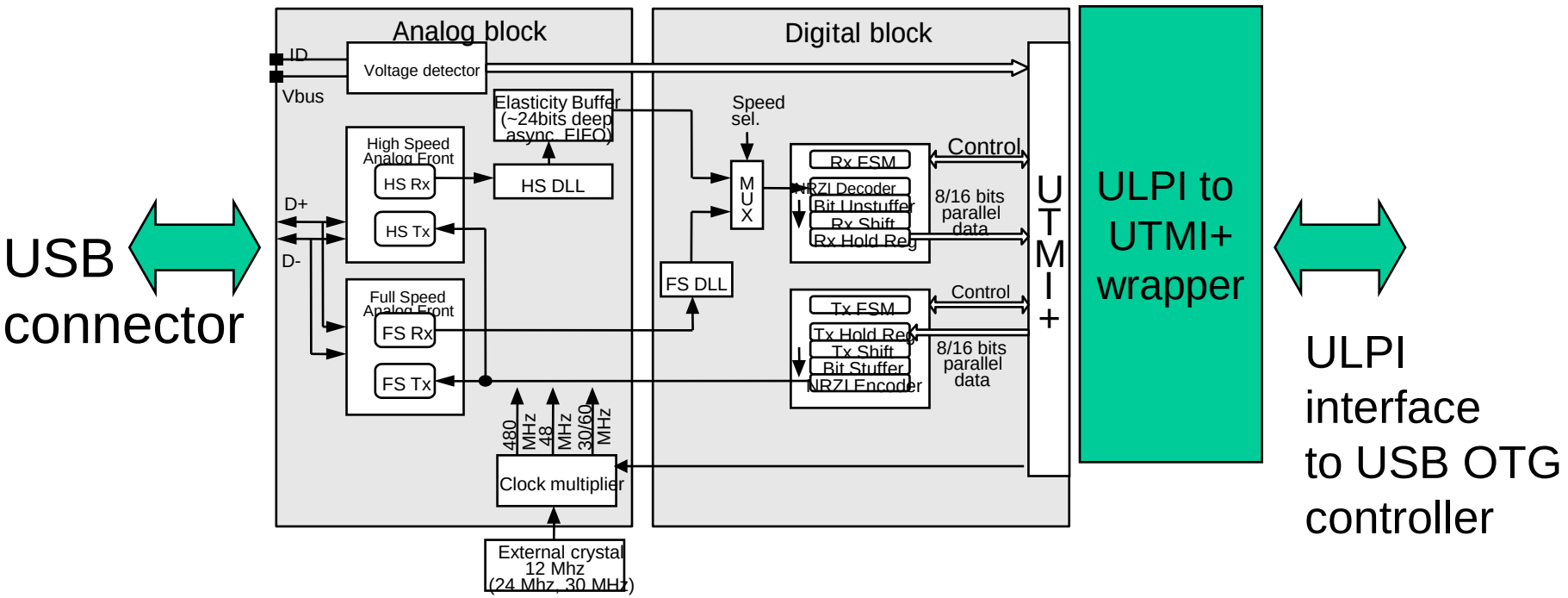
BS view of advICo Business Objectives



Ideas about exploitation of MAPPER results (product)

- USB OTG PHY as a product (hard IP core)
  - problems with technology dependence
  - possible distribution through silicon foundry
- Development of a chip
  - adding ULPI wrapper (tranceiver chip)
  - adding USB OTG controller and microcontroller

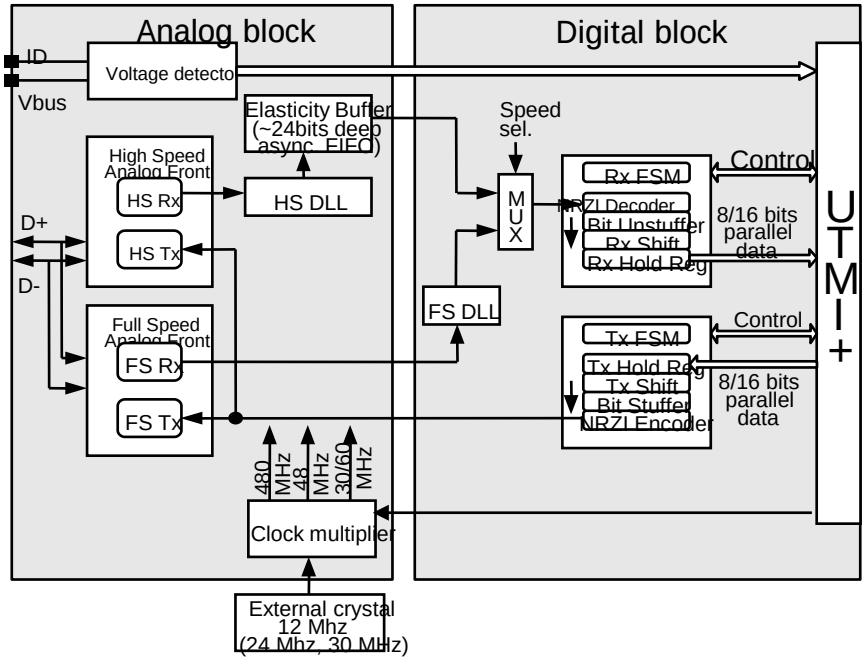
IP-based SoC design - Product (tranceiver chip)



IP-based SoC design - Product (microcontroller chip with USB interface)

Microcontroller interface

USB connector



USB OTG controller

R8051XC micro-controller core

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- Development of a chip
  - adding ULPI wrapper (tranceiver chip)
  - adding USB OTG controller and microcontroller
- Business discussion between Evatronix & advICo already started in parallel to technical work

Ideas about exploitation of MAPPER results (processes)

- Elaboration of the notion of *extended product* in the context of IP cores (suggested by CIEL)
  - Support for organizational change at Evatronix leading from *project-oriented* (focus on engineering) to *product-oriented* (focus on marketing) management
  - In-line with activities within 6FP SPRINT project (in cooperation with Philips, STMicorelectronics and Infineon, adding additional views to today state-of-the-art deliverable set for IP cores)
- Use of CIEL results in definition of formal model of distributed collaboration & supporting tools
  - setting up partnerships in design outsourcing
- Use of process models and balanced scorecard(s) (previously mentioned) developed during MAPPER for improvement of our business practices
- Interest in Mapper WP4 results – multi project management
  - planned implementation of MS Project server based EPM (enterprise project management) system in Q4'2006, but formal methodology knowledge missing