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Analog Design Flow

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Analog Design Flow

- Most analog/RF designs are of small complexity (<10k devices)
- Optimum analog performance requires individual optimization of every single device
- Process tolerance (±20%) requires robust design (corner analysis, Monte-Carlo-Analysis)
- Simulation must be done with accurate SPICE models (BSIM3V3: >150 parameters per MOS device, VBIC: >90 parameters per BJT/HBT device)
- Mixture of low and high frequencies, long settling times of regulators etc. may cause long simulation times and huge output files
- System-level simulations may be accelerated by using analog hardware description languages (A-HDL)
- No automated process for HDL model generation...tradeoff between computing time and engineering time

Analog Design Flow

- Performance strongly affected by layout parasitics, effects must be determined by parasitic extraction and post-layout-simulation
- Noise coupling, thermal gradients, crosstalk etc. require careful manual layout (shielding in metallization and in silicon bulk, use cross-coupled pairs, etc.)
- Minimizing device mismatch requires placement of dummy devices and use of certain tricks (like multi-finger transistors)
- In effect: manual optimization and placement of all individual components
- Post-layout-simulation can be extremely time-consuming due to huge number of parasitic elements. Rule of thumb for bipolar designs: speed penalty 20..25%, power penalty up to 50%. CMOS worse
- Initial schematic design should be designed to operate on 125% target speed

Analog Design Flow

- Regularity and hierarchy in design helps to reduce design effort
- Reusability of analog designs very limited
  - Different devices with different properties in different technologies lead to full redesign cycle for every process
  - Different design rules lead to new manual layout process
  - Design requirements vary largely between different applications
- Testability in analog circuits sometimes difficult due to negative impact of test measures on the performance. Every circuit needs individual strategy what can be tested and how
- Analog IP (intellectual property) has limited lifetime (process lifetime) and limited market. Customized IP is an interesting intermediate between full-custom ASIC and pure IP design

Design Environment

- Work with UNIX (Linux and Solaris)
- Cadence Virtuoso flow for full-custom IC design
  - Schematic Composer for design entry
  - Spectre, Spectre/RF for SPICE-like and A-HDL simulation
  - Virtuoso/Virtuoso XL for full-custom layout (heretically: „polygon pusher“)/schematic driven layout
  - Diva/Assura for design verification (design rule check, electrical rule check, layout versus schematic) and for parasitic extraction (parasitic resistance and capacitance, mostly)
  - Hierarchy editor for post-layout simulation (replace selected subcircuit schematics with extracted netlists)
- Standard UNIX tools like octave for some postprocessing
- Self-written UNIX tools for modelling of striplines and inductors

Design Methodology

- Evaluation of a target specification, based on customers demand
- Manufacturing process selection
- Architecture development, discussion of alternatives
- Environmental issues (housing/PCB/ESD), system testbench
- System simulation, if necessary (A-HDL)
- Partition in subblocks
- Integrate testability
- Initial subblock design, derivation of subblock specs, documentation
- Review of architecture, interface specification (between blocks)
- Subblock optimization with
  - Corner analysis, Monte-Carlo
  - Post-layout-simulation
- Simulation of complete circuit, documentation
- Design verification, stream-out, tape-out

Design Methodology

- Specification of an analog subblock not trivial due to huge number of variables and time-consuming simulations
- Interface between circuit blocks not as easy as in digital domain
- Issues to handle:
  - Load (Sink/Source)
  - Crosstalk/Isolation/Noise
  - Levels (Voltage/Current)
  - Standby-conditions (pull-up/pull-down/float)
  - Power (avoid additional devices if possible)
  - Stability (parasitic inductance, reflections, neg. resistance)
- Strong interaction between the designers necessary to avoid time-consuming mistakes and to identify critical parts of the design ASAP

WP2 Design: Universal Serial Bus - USB2

- Serial data stream with up to 480 Mbit/s on the bus
- „low speed“ makes pure CMOS design possible, thus integration of analog interface and logic on single chip is possible
- Interface to USB Transceiver Macrocell (UTM) with 16bit/30MHz or 8bit/60MHz allows VHDL design & synthesis of digital part
- Complex USB specification (~1000 pages) divides (analog/high-speed) UTM part and low-speed digital part, e.g. SIE (serial interface engine), OTG (on-the-go) or device-specific logic
- The UTMI (UTM Interface) specifies the interface between the high-speed/analog and the digital part, allowing separate design methodologies and/or manufacturing technologies (e.g. UTM/PHY ASIC and SIE gate array)
- UTM specification simplifies reuse of design due to clear interface specification

WP2 Design: USB2

- Challenges in USB2 UTM design:
  - Huge tolerances of CMOS processes require measurement/calibration techniques to meet specification
  - Integration of logic speaks for modern sub-µm process, but on the other hand 5V-tolerant I/O is mandatory. Technology with dual gate-oxide needed for a fully integrated design?
  - Most circuitry in the UTM is digital, but frequencies of 480 MHz and asynchronous logic is difficult to handle with digital tools?
  - Complexity of UTM may require more HDL throughout the design than we usually do. How accurate are the models?
- Integrity of entire design
  - Integration and verification of design data from analog and digital part with data from different design tools...full-chip LVS?
  - Simulation of complete system?